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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/625,643	07/25/2000	Noriaki Hiraga	052593-5003	7356

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EXAMINER	
KITOV, ZEEV	
ART UNIT	PAPER NUMBER
2836	

DATE MAILED: 11/04/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/625,643	HIRAGA, NORIAKI	
	Examiner	Art Unit	
	Zeev Kitov	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 July 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 11, 15, 16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) *12 - 14, 17 - 45* are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. Claims 12 – 14 and 17 – 45 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to non elected embodiments, there being no allowable generic or linking claim. Election was made **without** traverse in Paper No. 5. Applicant elected claims 1 – 11, 15 and 16 for prosecution.

Objections

2. Claims 1 and 5 are objected to due to a following misspelling: the word "difference" should be replaced by the word "different". Appropriate correction is required.

3. Claim 2 is objected to due to a following misspelling: "multiplicity of basic cells for active elements regularly arranged in repetition". Examiner's opinion is that the word "for" should be replaced by "of". Additionally, the word "multiplicity" should be replaced by "plurality".

4. Claim 1 is objected to due to a lack of antecedent basis for a statement. Claim recites in line 9 the following limitation: "another connection configuration", which assumes existence of antecedent basis. There is insufficient antecedent basis for this limitation in the claim. Appropriate correction is required.

5. Specification is objected to due to multiple errors. For example, on page 6, line 16, "the output element 12B" should be replaced by "input element 12B", on page 9,

line12, "a black circuit in Fig. 11D" should be replaced by "a black line in Fig. 11D". Substantial check-up and rewriting are required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

5. Claims 5 – 11, 15 and 16 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. A reason for that is that the Claim 5 recites a second connection configuration (line 16) and the first connection configuration (lines 19, 20). It is not clear from the text whether the "said active element" of line 20 has connection of the first or the second configuration. In general, an exact meaning of Claim 5 limitations is unclear.

6. Claim 15 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite and failing to conform to current U.S. practice. It appears to be a literal translation into English from a foreign document and is replete with grammatical and idiomatic errors. An exact meaning of the following statement (lines 12 – 13): "said active elements in the third connection configuration <u>are arranged instead of or exclusively of said active element</u> (emphasized by Examiner) in the second connection configuration", is unclear. For purpose of examination it was assumed that the active element in the third

connection configuration replaced the active element of the second connection configuration.

An examination of Claims 5 – 11, 15 and 16 was performed based on the examiner's best interpretation of the claims in light of the 35 USC 112, 2nd paragraph rejection.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1, 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watt, US Patent 5,623,156, in a view of Yu, US Patent 5,361,185.

Watt discloses most of the elements of Claim 1, including circuit having different power lines (elements Vdd0 and Vdd1 in Fig. 5), a signal wire connecting the circuits (I/O PAD implicitly suggests interconnecting wire between IC's in Fig. 5), active elements in another connection configuration (element M0 in Fig. 5) having a structure similar to that of the elements in a first connection configuration (both are MOS transistors) being arranged near the active element in the first connection configuration (bottom part of element 12 in Fig. 5). The element in the first connection configuration is connected to the inter-circuit signal wire (through element R to I/O PAD in Fig. 5),

while the elements in another connection configuration are connected to power lines (element M0 connected to Vssi and indirectly to Vsso in Fig. 5) and isolated from signal wires (of internal protected circuitry not shown in Fig. 5) other than the inter-circuit signal wire (I/O PAD in Fig. 5). However Watt does not disclose the spatial placement of the active elements with respect to the protected active elements. Yu discloses plurality of active elements (transistors) arranged near the active element in the first connection configuration connected to the inter-circuit signal wire (Claim 1, col. 6, lines 34 – 44, 45 – 49).). Yu further discloses that the active elements of the first and another configurations must be placed in close proximity (col. 5, lines 59 – 64), because in that case they respond to the ESD event faster than in a case of the remote clamps.

Both patents have the same problem solving area, namely providing efficient ESD protection to semiconductor equipment. Therefore it would have been ordinary skill in the art at the time the invention was made to have used multiple circuit mounted in the same circuit forming region (wafer), because of well known in the art modern tendency for miniaturization leading to increase of package density of the IC's.

Regarding Claim 3, Yu discloses IC device having a substrate formed in a single chip (see Fig. 6) and the circuit-forming region is allocated to one surface of the substrate (Fig. 6, 7, 8a and 8b).

Regarding Claims 4, Watt discloses the circuit-forming region including signal input/output circuits (elements 14, 28 and in Fig. 5), and external connection terminals outside the input/output circuits (I/O PAD in Fig. 5).

8. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Watt, US Patent 5,623,156, in a view of Yu, US Patent 5,361,185, and further in a view of Ker, US Patent 6,075,686.

As was stated above, Watt and Yu disclose all the elements of Claim1. But regarding Claim 2, they do not disclose the internal cells including multiple basic cells of active elements arranged in repetition and the active element in the first connection configuration and the active element in the second connection configuration are allocated to some of the basic cells. Kerr implicitly discloses the internal cells including multiple basic cells of active elements arranged in repetition and the active element in the first connection configuration and the active element in the second connection configuration are allocated to some of the basic cells. As well known in the art, modern integrated circuits, especially digital IC's, are formed as plurality of basic cells of active elements arranged in repetition. Therefore Circuit I, Circuit II and Circuit III, being digital integrated circuit, must be formed this way, i.e. each basic cell must have allocated active elements in the first connection configuration, i.e. must have MOS transistors (element 12 in Fig. 5 of Watt) and according to Yu (col. 5, lines 59 – 64), the protection elements should be allocated in close proximity to the protected element.

All the cited references have the same problem solving area, namely providing efficient ESD protection for semiconductor equipment. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used multiple basic cells arranged in repetition and each cell being provided with active elements of the first connection configuration and the second connection configuration,

because it must have MOS transistors (element 12 in Fig. 5 of Watt) as the active element in the first connection configuration and according to Yu (col. 5, lines 59 – 64), the protection elements should be allocated in close proximity to the protected element.

9. Claims 5 - 11, 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watt, US Patent 5,623,156, in a view of Yu, US Patent 5,361,185 and further in a view of Staab, US Patent 5,610,790.

Watt discloses most of the elements of Claim 5, including circuit having different power lines (elements Vdd0 and Vdd1 in Fig. 5), a signal wire connecting the circuits (I/O PAD implicitly suggests interconnecting wire between IC's in Fig. 5), active elements in a second connection configuration (element 22 in Fig. 5). The first connection configuration is presented by element 12 in Fig. 5. The element in the first connection configuration is connected to the inter-circuit signal wire (through element R to I/O PAD in Fig. 5), while the elements in the second connection configuration are connected to power lines and isolated from signal wires and other circuit signal wires. However Watt does not disclose the spatial placement of the active elements with respect to the protected active elements, neither he discloses an exact structure of the core clamp (element 22). Yu discloses plurality of active elements (transistors) arranged near the active element in the first connection configuration connected to the inter-circuit signal wire (Claim 1, col. 6, lines 34 – 44, 45 – 49).). Yu further discloses that the active elements of the first and another configurations must be placed in close proximity (col. 5, lines 59 – 64), because in that case they respond to the ESD event faster than in a

case of the remote clamps. Both patents have the same problem solving area, namely providing efficient ESD protection to semiconductor equipment. Therefore it would have been ordinary skill in the art at the time the invention was made to have used multiple circuit mounted in the same circuit forming region (wafer), because of well known in the art modern tendency for miniaturization leading to increase of package density of the IC's.

Staab discloses an exact structure of the supply lines clamp. A cross power supply clamp 716 in Fig. 7 is the element of a similar structure to the active element (element 12 in Fig. 5 of Watt) in the first connection configuration (both include FET transistors). Both patents have the same problem solving area, namely providing efficient ESD protection to semiconductor equipment. Therefore it would have been ordinary skill in the art at the time the invention was made to have used MOSFET transistor as an inter-power supply clamp in the circuit of Watt, because as Staab states (col. 3, lines61 – 67, col. 4, lines1 – 35), there is a need for protection of the voltage supply rails against ESD events.

Regarding Claim 6, Yu discloses the active elements of the first and another configurations must be placed in close proximity (col. 5, lines 59 – 64).

Regarding Claim 8, Yu discloses IC device having a substrate formed in a single chip (see Fig. 6) and the circuit-forming region is allocated to one surface of the substrate (Fig. 6, 7, 8a and 8b).

Regarding Claim 9, Watt discloses the circuit-forming region including signal input/output circuits (elements 14, 28 and in Fig. 5), and external connection terminals outside the input/output circuits (I/O PAD in Fig. 5).

Regarding Claim 10, Yu discloses an active element in a third connection configuration (elements Q1 – Q4 in Fig. 1) including element of similar structure to the active element in the first connection configuration (MOS transistors are similar to those used in element 12, Fig. 5 of Watt), connected to power lines of an internal circuit (elements Vcc and Vss in Fig. 1 of Yu) and the inter-circuit signal wire (between PAD and INTERNAL CKT) and being isolated from other signal lines.

Regarding Claim 11, Yu discloses the active elements of the first and another configurations must be placed in close proximity (col. 5, lines 59 – 64).

Regarding Claim 15, Yu discloses placement of the protection elements in close vicinity of the protected circuit. According to him, the active elements of the first and another configurations must be placed in close proximity (col. 5, lines 59 – 64). Yu discloses a protection element protecting a reception side of the circuit. Therefore in combined circuit of Watt, Yu and Staab the protecting element of Yu will be protecting the reception side of the inter-circuit signal wire in the other (second one) of the pair of internal circuits.

Regarding Claim 16, Yu discloses the active elements of the first and another configurations must be placed in close proximity (col. 5, lines 59 – 64). Therefore, placing elements of the first circuit configuration to sandwich the active element of the first connection configuration is a natural way design of the modern IC's, when due to

increasing packaging density the same type elements locate in close vicinity, sandwiching each other. As to placement of elements of the second and third connection configuration sandwiching the elements of the first connection configuration, since elements of the second and third circuit configurations are protective circuits, according to Yu, they should be placed in close vicinity sandwiching the protected circuit in the first connection configuration (element 12 in Fig. 5 of Watt).

10. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Watt in a view of Yu, Staab and Ker, US Patent 6,075,686.

As was stated above, Watt, Yu and Staab disclose all the elements of Claim 5. But regarding Claim 7 they do not disclose the internal cells including multiple basic cells of active elements arranged in repetition and the active element in the first connection configuration and the active element in the second connection configuration are allocated to some of the basic cells. Kerr implicitly discloses the internal cells including multiple basic cells of active elements arranged in repetition and the active element in the first connection configuration and the active element in the second connection configuration are allocated to some of the basic cells. As well known in the art, modern integrated circuits, especially digital IC's, are formed as plurality of basic cells of active elements arranged in repetition. Therefore Circuit I, Circuit II and Circuit III, being digital integrated circuit, must be formed this way, i.e. each basic cell must have allocated active elements in the first connection configuration, i.e. must have MOS

transistors (element 12 in Fig. 5 of Watt) and according to Yu (col. 5, lines 59 – 64), the protection elements should be allocated in close proximity to the protected element.

All the cited references have the same problem solving area, namely providing efficient ESD protection for semiconductor equipment. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used multiple basic cells arranged in repetition and each cell being provided with active elements of the first connection configuration and the second connection configuration, because it must have MOS transistors (element 12 in Fig. 5 of Watt) as the active element in the first connection configuration and according to Yu (col. 5, lines 59 – 64), the protection elements should be allocated in close proximity to the protected element.

Conclusion

The prior art made of record not relied upon is considered pertinent to applicant's disclosure

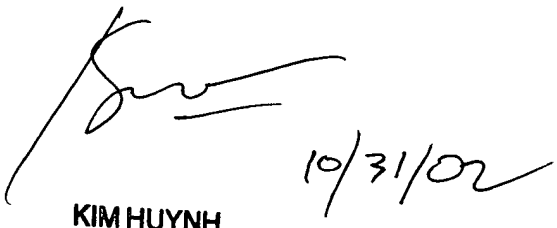
- US Patent 5,237,395 – Power rail ESD protection circuit – Lee,
- US Patent 6,144,542 – ESD bus lines in CMOS IC's for whole-chip ESD protection – Ker,
- US Patent - 6,353,520 – Shared 5 volt tolerant ESD protection circuit for low voltage CMOS process – Andersen et al.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zeev Kitov whose telephone number is (703) 305-0759. The examiner can normally be reached on 8:00 – 4:30.

If attempts to reach examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on (703) 308-3119. The fax phone numbers for organization where this application or proceedings is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Z.K.
10/31/02



KIM HUYNH
PRIMARY EXAMINER